CLAIMS

1. A method for forming structures self-aligned with each other on a semiconductor substrate, comprising the following steps:

forming, on the semiconductor substrate, first regions of a first material projecting from said semiconductor substrate;

forming, on the whole of said semiconductor substrate, a protective layer of a second material, said second material being selective with respect to said first material;

removing said protective layer to expose said first regions through a planarizing step,;

etching said first regions to expose said semiconductor substrate, and forming second regions projecting from the substrate of said protective layer.

2. A method for forming structures self-aligned with each other according to Claim 1, characterized in that it comprises the following steps:

forming first spacers of a second selective material with respect to the first material on the sidewalls of said first regions, before said protective layer is formed.

3. A method for forming structures self-aligned with each other according to Claim 2, characterized in that it comprises the following steps:

etching said first regions to expose said semiconductor substrate, and forming regions projecting from the substrate of said protective layer.

4. A method for forming structures self-aligned with each other according to Claim 1, characterized in that it comprises the following steps:

carrying out an implanting step on the whole semiconductor substrate to form, on said semiconductor substrate, first implanted regions adjacent to said first regions, before the protective layer is formed.

5. A method for forming structures self-aligned with each other according to Claim 1, characterized in that it comprises the following steps:

carrying out an implanting step on the whole of said semiconductor substrate to form, on said semiconductor substrate, implanted regions adjacent to said second regions.

6. A method for forming structures self-aligned with each other according to Claim 2, characterized in that it comprises the following steps:

forming second spacers on the sidewalls of said first spacers.

7. A method for forming structures self-aligned with each other according to Claim 2, characterized in that said first spacers are made of a third material selective with respect to the first material.

8. A method for forming structures self-aligned with each other according to Claim 6, characterized in that said second spacers are made of a fourth material selective with respect to the first material.

9. A method for forming structures self-aligned with each other according to Claim 1, characterized in that said planarizing step is carried out by using a CMP technique.

10. A method for forming structures self-aligned with each other according to Claim 1, characterized in that said first material is a silicon oxide and said second material is silicon nitride.

11. A method for forming structures self-aligned with each other according to Claim 1, characterized in that said first material is silicon nitride and said second material is a silicon oxide.

12. A method for forming structures self-aligned with each other according to Claim 1, characterized in that it comprises the following steps:

forming an additional protective layer on the whole of said substrate before forming said first regions of a fifth material selective with respect to the first

material.

13. A method for forming structures self-aligned with each other according to Claim 8, characterized in that said third and fourth materials are silicon nitride.

14. A method for forming structures self-aligned with each other according to Claim 8, characterized in that said fifth material is silicon oxide.

15. A method for forming structures self-aligned with each other according to Claim 1, characterized in that said first implanted regions are extrinsic base regions of a bipolar transistor, and that said at least second regions are bipolar transistor emitter and base junctions, respectively.

16. A method for forming structures self-aligned with each other according to Claim 2, characterized in that it comprises the following steps:

forming, on said semiconductor substrate, a metal layer after said first spacers are formed, and subsequent thermal treatment to selectively form a silicide layer on the substrate portions, that are exposed from said first regions, and said first spacers.

17. A method for forming structures self-aligned with each other on a semiconductor substrate, comprising the following steps:

forming, on the semiconductor substrate, first regions of a first material projecting from said semiconductor substrate;

forming first spacers of a second selective material with respect to the first material on the sidewalls of said first regions, before said protective layer is formed;

forming, over the whole of said semiconductor substrate, a protective layer of a third material selective with respect to the second material;

removing said protective layer to expose said first regions through a planarizing step;

etching said first spacers to expose said semiconductor substrate, and forming regions projecting from the substrate of said protective layer.

18. A method of forming self-aligned structures in a semiconductor substrate, the method comprising:

forming first regions of a first material on a surface of the semiconductor substrate;

forming second regions in exposed portions of the semiconductor substrate, the exposed portions being defined by the first regions of the first material;

forming on the first regions and on the exposed portions of the semiconductor substrate third regions of a second material, the second material being selectively removable relative to the first material;

removing portions of the second material to expose the first regions;

removing the first regions to expose corresponding portions of the semiconductor substrate; and

forming fourth regions in the exposed portions of the semiconductor substrate.

19. The method of claim 18 wherein forming first regions further comprises forming spacers on sidewalls of the first regions, the spacers being formed from a third material and having a thickness to define a desired distance between each fourth region and adjacent second regions.

20. The method of claim 18 further comprising:

prior to forming the fourth regions, forming spacers on sidewalls of the third regions, the spacers having a thickness to define a width of the fourth regions subsequently formed.

21. The method of claim 20 wherein the first, second and third regions have dimensions limited by an associated photo lithographic process, and wherein the thickness of the spacers defines widths of the fourth regions that are less than a minimum dimension of the photo lithographic process.

22. The method of claim 18 wherein the first material comprises silicon dioxide and wherein the second material comprises silicon nitride.

23. The method of claim 18 wherein removing portions of the second material comprises planarizing the second material to expose the first regions.

24. A semiconductor device in a semiconductor substrate, the device including a plurality of regions being formed using an associated photo lithographic process having a minimum dimension of such regions, the device comprising:

first regions in the semiconductor substrate; and

second regions in the semiconductor adjacent the first regions, the second regions having dimensions less than the minimum dimension of the associated photo lithographic process.

25. The semiconductor device of claim 24 wherein the device comprises a bipolar transistor, and wherein adjacent first regions form a base region of the transistor and a second region formed between these first regions forms an emitter of the transistor.

26. A semiconductor integrated circuit including a device, the device comprising:

a plurality of first regions formed using an associated photo lithographic process, the photo lithographic process defining a minimum dimension of such regions; and

second regions adjacent the first regions, the second regions having dimensions less than the minimum dimension of the associated photo lithographic process.

27. The semiconductor integrated circuit of claim 26 wherein the integrated circuit comprises a memory device.

28. An electronic system including a semiconductor integrated circuit, the semiconductor integrated circuit comprising:

a semiconductor device including,

a plurality of first regions formed using an associated photo lithographic process, the photo lithographic process having a minimum dimension of such regions; and

second regions adjacent the first regions, the second regions having dimensions less than the minimum dimension of the associated photo lithographic process.

29. The electronic system of claim 28 wherein the electronic system comprises a computer system.